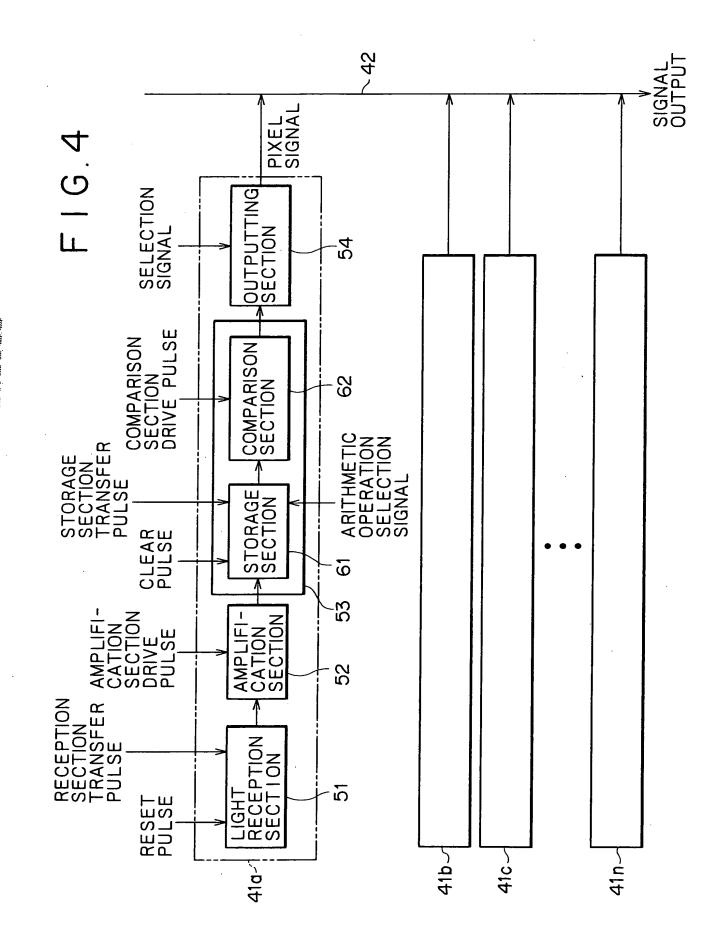
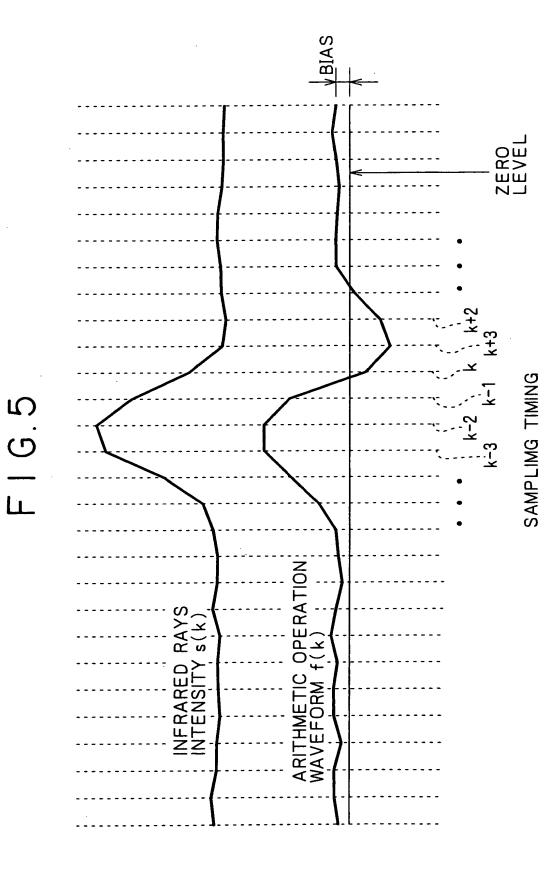
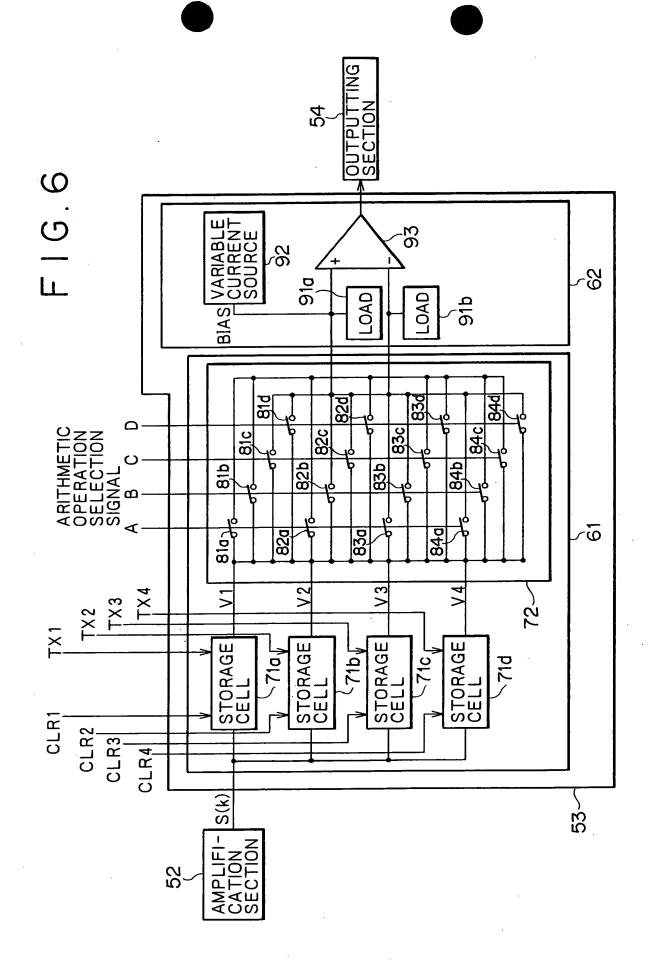


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## F I G.7

START

S<sub>1</sub>

PATTERN LIGHT IS IRRADIATED, AND LIGHT FROM IMAGING OBJECT 2 IS CONDENSED BY LENS 13 AND INTRODUCED INTO PRISM 14

**S2** 

LIGHT IS SPECTRALLY SEPARATED INTO VISIBLE RAYS AND INFRARED RAYS BY PRISM 14, AND INFRARED RAYS ARE OUTPUTTED TO DISTANCE SENSOR 17 WHILE VISIBLE RAYS ARE OUTPUT TO IMAGER 15

S3

VISIBLE RAYS ARE INPUTTED TO IMAGER 15, FROM WHICH COLOR INFORMATION IS OUTPUTTED TO VIDEO SIGNAL PROCESSING SECTION 16.

VIDEO SIGNAL PROCESSING SECTION 16 PERFORMS GAIN ADJUSTMENT AND COLOR SIGNAL PROCESSING AND OUTPUTS COLOR VIDEO SIGNAL TO COMPUTER 19.

OUTPUTS COLOR VIDEO SIGNAL TO COMPUTER 19.
INFRARED RAYS ARE PROCESSED BY DISTANCE SENSOR
17 AND OUTPUTTED AS BINARY DIGITIZED SIGNAL TO
SHAPE DATA PROCESSING SECTION 18, AND SHAPE DATA
PROCESSING SECTION 18 CALCULATES AND OUTPUTS
DISTANCE TO COMPUTER 19.

**S4** 

COMPUTER 19 PERFORMS COMPUTER GRAPHICS PROCESSING FOR COLOR VIDEO SIGNAL AND SHAPE DATA AND OUTPUTS RESULTING DATA TO MONITOR 3 OR EXTERNAL STORAGE APPARATUS 4

END

FIG.8

START

S11

INFRARED RAYS ARE RECEIVED BY LIGHT RECEPTION SECTION 51 IN SYNCHRONISM WITH RESET PULSE FROM TIMING GENERATOR 32

S12

RECEIVED INFRARED RAYS ARE PHOTOELECTRICALLY CONVERTED AND OUTPUTTED TO AMPLIFICATION SECTION 52 IN SYNCHRONISM WITH LIGHT RECEPTION SECTION TRANSFER PULSE FROM TIMING GENERATOR 32

S13

SIGNAL INPUTTED TO AMPLIFICATION SECTION 52 IS AMPLIFIED AND OUTPUTTED TO ARITHMETIC OPERATION SECTION 53

**S14** 

ARITHMETIC OPERATION SECTION 53 ERASES STORAGE OF STORAGE CELL 71a IN SYNCHRONISM WITH CLEAR PULSE CLR1 FROM HORIZONTAL SCANNING CIRCUIT 33a, AND STORES SIGNAL FROM AMPLIFICATION SECTION 52 INTO STORAGE CELL 71a IN SYNCHRONISM WITH NEXT STORAGE SECTION TRANSFER PULSE

S15

STORAGE CELLS 71a TO 71d OUTPUT SIGNALS STORED THEREIN TO MATRIX CIRCUIT 72

**S16** 

MATRIX CIRCUIT 72 SWITCHES ON SWITCHES 81a TO 84a IN RESPONSE TO SIGNAL OF MODE A OF ARITHMETIC OPERATION SELECTION SIGNAL FROM ARITHMETIC OPERATION CONTROL SECTION 35, AND OUTPUTS THOSE ONES V1 AND V2 OF OUTPUTS OF STORAGE CELLS 71a TO 71d TO POSITIVE INPUT OF DIFFERENTIAL AMPLIFICATION CIRCUIT 93 OF THE COMPARISON SECTION 62 AND THOSE ONES V3 AND V3 OF OUTPUTS TO NEGATIVE INPUT

S17

BIAS FROM VARIABLE CURRENT SOURCE 92 IS INPUTTED ADDITIONALLY TO POSITIVE INPUT OF DIFFERENTIAL AMPLIFICATION CIRCUIT 93, AND INPUTS TO POSITIVE AND NEGATIVE INPUTS OF DIFFERENTIAL AMPLIFICATION CIRCUIT 93 ARE COMPARED WITH EACH OTHER.

RESULT OF COMPARISON IS OUTPUTTED TO OUTPUTTING SECTION 54

S18

OUTPUTTING SECTION 54 OUTPUTS COMPARISON RESULT AS PIXEL SIGNAL TO OUTPUTTING CIRCUIT 34 OVER COMMON SIGNAL LINE 42

S19

PIXEL SIGNAL INPUTTED TO OUTPUTTING CIRCUIT 34 IS OUTPUTTED TO SHAPE DATA PROCESSING SECTION 18

END

